(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 692 824 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
17.01.1996 Bulletin 1996/03

(51) Int. Cl.[6]: **H01L 23/522**

(21) Application number: **95111148.3**

(22) Date of filing: **14.07.1995**

(84) Designated Contracting States:
DE FR GB IT NL

(30) Priority: **15.07.1994 US 275570**

(71) Applicant: **TEXAS INSTRUMENTS INCORPORATED**
Dallas, Texas 75243 (US)

(72) Inventors:
- **Numata, Ken**
  Dallas, TX 75240 (US)
- **Houston, Kay L.**
  Richardson, TX 75080 (US)

(74) Representative: **Brown, Angela Mary et al**
Sunbury on Thames, Middlesex TW16 7AX (GB)

(54) Improvements in and relating to semiconductor devices

(57) A semiconductor device (and method of manufacturing thereof) having metal leads **(114+130)** with improved reliability, comprising metal leads **(114+130)** on a substrate **112**, a low-dielectric constant material **(116)** at least between the metal leads **(114+130)**, and dummy vias **(122+134)** in contact with the metal leads **(114+130)**. Heat from the metal leads **(114+130)** is transferable to the dummy vias **(122+134)**, and the dummy vias **(122+134)** are capable of conducting away the heat. The low-dielectric constant material **(116)** may have a dielectric constant of less than about 3.5. An advantage of the invention is to improve reliability of metal leads in circuits using low-dielectric constant materials, especially in scaled-down circuits that are compact in the horizontal direction.

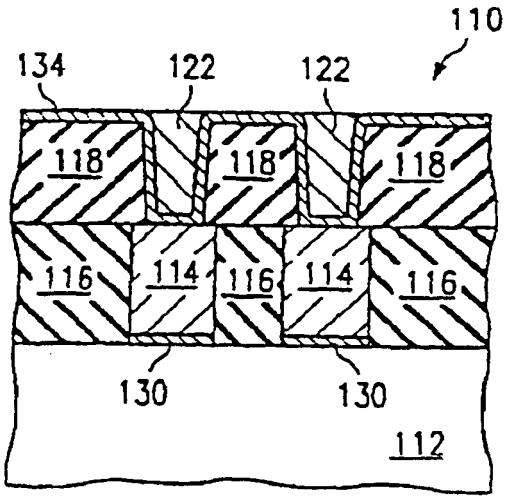

FIG. 3B

EP 0 692 824 A2

Description

Field of the Invention

This invention relates generally to the fabrication of semiconductor devices, and more specifically to semiconductors with submicron spacing (where the conductor width and the conductor-to-conductor spacing are both less than one micron) and low-dielectric constant materials between intermetallic leads.

Background of the Invention

Semiconductors are widely used in integrated circuits for electronic applications, including radios and televisions. Such integrated circuits typically use multiple transistors fabricated in single crystal silicon. Many integrated circuits now contain multiple levels of metallization for interconnections.

Semiconductor devices are being scaled down in the horizontal dimension to reduce wafer cost by obtaining more chips per wafer or by increasing circuit complexity by obtaining more transistors per chip. Although semiconductor devices are being scaled down in the horizontal dimension, semiconductor devices are not generally being scaled down in the vertical dimension (because the current density would exceed reliability limits). Thus, conductors may have a high aspect ratio (ratio of conductor height to conductor width of greater than one). With horizontal scaling, these tall metal leads are being packed closer and closer together, causing capacitive coupling between the leads to become the primary limitation to circuit speed. If line-to-line capacitance is high, a likelihood for electrical inefficiencies and inaccuracies exist. Reducing the capacitance within these multi-level metallization systems will reduce the RC time constant between the lines.

Typically, the material used to isolate metal lines from each other is silicon dioxide. However, the dielectric constant of dense silicon oxide grown by thermal oxidation or chemical vapor deposition is on the order of 3.9. The dielectric constant is based on a scale where 1.0 represents the dielectric constant of a vacuum. Various materials exhibit dielectric constants from very near 1.0 to values in the hundreds.

Summary of the Invention

Recently, attempts have been made to use low-dielectric constant materials to replace silicon dioxide as a dielectric material. The use of low-dielectric constant materials as insulating layers reduces the capacitance between the conductors (or metal leads), thus reducing the RC time constant. It has been found that using materials with dielectric constants less than about 3.5 sufficiently reduces the RC time constant in typical submicron circuits. As used herein, the term low-dielectric will refer to a material with a dielectric constant of less than about 3.5.

One problem herein is that the decreased thermal conductivity of low-dielectric constant materials, especially in circuits with high aspect ratio metal leads, may result in metal lead breakage due to the effects of Joule's heat. The present invention solves this problem by improving the thermal conductivity of the structure, resulting in improved reliability of conductors in structures using low-dielectric constant materials.

According to the present invention there is provided a method for forming conductors on a semiconductor device comprising, forming a conductor on a substrate, depositing a low-dielective layer over the conductor, and forming a dummy via in contact with said conductor, wherein heat from said conductor is transferable to said dummy via and conducted away from said conductor.

The present invention encompasses a semiconductor device structure (and method for manufacturing thereof) having conductors with improved reliability, comprising conductor on a substrate, a low-dielectric constant material between the conductors, and dummy vias in contact with the conductors. Heat from the conductors is transferable to the dummy vias, which are capable of thermally conducting the heat away from the conductors. The low-dielectric constant material has a dielectric constant of less than about 3.5. An advantage of the invention is improved reliability of conductors for circuits using low-dielectric constant materials.

Another embodiment of a method according to the present invention comprises depositing an interconnect layer on a substrate, etching the interconnect layer in a predetermined pattern to form conductors, depositing a low-dielectric constant material between the conductors, depositing an insulating layer over the low-dielectric constant material and the tops of the conductors, etching the insulating layer to leave channels in the insulating layer abutting the tops of the conductors, and depositing a metal layer over the insulating layer to fill the channels and form dummy vias in contact with the tops of the conductors.

According to a further embodiment of the present invention there is provided a semiconductor device comprising a conductor formed on a substrate, a dummy via in contact with said conductor, wherein heat from said conductor is transferable to said dummy via, and said dummy via is capable of conducting heat away from said conductor.

Another embodiment of the invention is a semiconductor device conductors with improved reliability, comprising a substrate, conductors on the substrate, a low-dielectric constant material between the conductors, and dummy vias in

contact with theconductors, wherein heat from the metal leads is transferable to the dummy vias, and where the dummy vias are capable of conducting away the heat from the conductors.

An advantage of the invention is improved reliability of conductors for circuits using low-dielectric constant materials. The invention is particularly beneficial to semiconductors having a combination of conductors with high aspect ratios and low-dielectric constant materials which are more thermally insulating.

Brief Description of the Drawings

In the drawings, which form an integral part of the specification and are to be read in conjunction therewith, and in which like numerals and symbols are employed to designate similar components in various views unless otherwise indicated:

Figures 1A-1C are three-dimensional views of a metal lead of a semiconductor wafer, showing the negative effects of Joule's heat;
Figures 2A-2D and **3A-3C** are cross-sectional elevational views of a first embodiment of the present invention, showing dummy vias formed in contact with metal leads on a semiconductor wafer to thereby avoid the negative effects of Joule's heat as depicted in **Figure 1**;
Figure 4 is a perspective view of a first embodiment of the invention generally illustrated in **Figure 3B**;
Figure 5 is a cross-sectional elevational view of a second embodiment of the present invention, with dummy vias in contact with both the top and bottom of metal leads;
Figure 6 is a perspective view of the second embodiment, generally illustrated in **Figure 5**;
Figure 7 is a cross-sectional elevational view of a third embodiment of the present invention, showing dummy vias formed in contact with metal leads on a semiconductor wafer, where the dummy vias are also in contact with dummy leads in another metal layer;
Figure 8 is a cross-sectional elevational view of a fourth embodiment, in which the vertical heat conduction path extends throughout the entire wafer;
Figure 9 is a cross-sectional elevational view of a fifth embodiment, which shows the use of a thermoconductive insulating layer; and
Figures 10A-10D and 11A-11C are cross-sectional elevational views of a sixth embodiment.

Detailed Description of Preferred Embodiments

The making and use of the presently preferred embodiments are discussed below in detail. However, it should be appreciated that the present invention provides many applicable inventive concepts which can be embodied in a wide variety of specific contents. The specific embodiments discussed are merely illustrative of specific ways to make and use the invention, and do not delimit the scope of the invention.

The following is a description of several embodiments of the present invention, including manufacturing methods. Corresponding numerals and symbols in the different figures refer to corresponding parts unless otherwise indicated. The text below provides an overview of the elements of the embodiments and the drawings.

Drawing Element 110, Semiconductor wafer is the generic term.
Drawing Element 112, Silicon (Substrate), may be other metal interconnect layers or semiconductor elements, (e.g., transistors, diodes); oxides; compound semiconductors (e.g., GaAs, InP, Si/Ge, SiC).
Drawing Element 114, Titanium trilayer (TiN/AlCu/TiN) (First metal interconnect portion of metal leads) is defined as Al, Cu, Mo, W, Ti, Si or alloys thereof; Polysilicon, silicides, nitrides, carbides; AlCu alloy with Ti or TiN underlayers; Metal interconnect layer.
Drawing Element 116, OSOG (organic spin-on glass) (Low-dielectric constant material) is defined as an air gap (also inert gases, vacuum); silica aerogel; other aerogels or xerogels; fluorinated silicon oxide.
Drawing Element 118, TEOS (tetraetho-xysilane) silicon dioxide (Insulating layer) is defeined as SiO_2; an insulating layer, typically an oxide and preferably having a thickness less than the height of metal leads **114**.
Drawing Element 119, Channels are holes in insulating layer **118** where dummy vias **122** will be formed
Drawing Element 120, Tungsten (metal layer) is defined as Titanium trilayer (TiN/AlCu/TiN); Cu, Mo, Al, Ti, Si or alloys thereof; Polysilicon, silicides, nitrides, carbides; AlCu alloy with Ti or TiN underlayers.
Drawing Element 122, Tungsten (Metal layer portion of dummy vias) is defined as Titanium trilayer (TiN/AlCu/TiN); Cu, Mo, Al, Ti, Si or alloys thereof; Polysilicon, silicides, nitrides, carbides; AlCu alloy with Ti or TiN underlayers.
Drawing Element 124, Aluminium alloy (Second metal interconnect portion of functional metal leads) is defined as Titanium trilayer (TiN/AlCu/TiN or TiN/AlCu/W); Cu, Mo, W, Ti, Si or alloys thereof; Polysilicon, silicides, nitrides, carbides; AlCu alloy with Ti or TiN underlayers; Metal interconnect layer.

Drawing Element 126, Aluminum alloy (Second Interconnect Portion of Dummy leads) is defined as Titanium trilayer (TiN/AlCu/TiN); Cu, Mo, W, Ti, Si or alloys thereof; Polysilicon, silicides, nitrides, carbides; AlCu alloy with Ti or TiN underlayers; Metal interconnect layer.

Drawing Element 128, AlN (Thermo-conductive insulating layer) Thermo-conductive insulating layer is defined as Si_3N_4; both AlN and Si_3N_4 (e.g., bilayer or trilayer of Si_3N_4/AlN/Si_3N_4); Insulative material with a thermal conductivity 20% larger than the thermal conductivity of low-dielectric constant material **116** and preferably 20% larger than SiO_2; annealed SiO_2

Drawing Element 130, Ti (First barrier portion of metal leads) is defined as TiN or other Ti alloy; Ti/TiN bilayer; Cu, Mo, W, Al, Si or alloys thereof.

Drawing Element 132, TEOS (tetraetho-xysilane) silicon dioxide (Thin insulating layer) is defined as other insulative material.

Drawing Element 134 Yi, (Second barrier portion of dummy vias or functional metal leads) is defined as bilayer of Ti/TiN; TiN or other Ti alloy; Cu, Mo, W, Al, Si or alloys thereof.

An apparently heretofore-unrecognized problem in semiconductor circuits, especially circuits having high aspect ratio conductors with low-dielectric constant material between conductors, is that the decreased thermal conductivity of low-dielectric constant materials may result in metal lead breakage due to the effects of Joule's heat. Generally, as the dielectric constant of a material decreases, the conductivity of the material is also decreased. Since all metals have a certain amount of electrical resistance, metal leads with current therethrough experience heat production proportional to I^2R (Joule's law). Such heat through a metal lead is known as Joule's heat. The Joule's heat will raise the metal lead's temperature if the heat is conducted away therefrom at a slower rate than it is produced.

As a metal lead heats locally in one portion along it, the resistance in that portion rises slightly (due to properties of the metal); causing the temperature in that portion to rise even more (although slightly). The higher temperature can increase lead resistance and still further increase the local heating. Thus, locally heated metal leads can be damaged or fractured. The thinner the metal lead, the weaker it is (which is particularly a concern in submicron circuits). The use of low-dielectric constant materials as insulative layers further presents a problem, for such materials generally have poor thermoconductivity. With the use of most low-dielectric constant materials, much more of the Joule's heat generated in metal leads of a circuit remains concentrated in the lead itself.

The effect of Joule's heat on a portion **114** of a metal lead is shown in Figures **1A-1C**. Figure **1A** shows a perspective view of metal lead of a semiconductor wafer (other portions of the wafer are not shown). The cross-section of the lead is typically rectangular-shaped, with the height being greater than the width (a high aspect ratio), because of scale-down. The metal lead has been scaled down in the lateral direction, but scale-down in the vertical direction is limited by electrical conductivity requirements of the circuit. When current flows through metal lead, the metal lead is heated. In reality, a metal lead has thin and fragile portions, causing uneven lead profiles. Such unevenness cannot be avoided because photolithography and etching processes of metal leads are not ideal. Electromigration, intensified by Joule's heat, causes the metal lead to first weaken, and then thin. Thin and fragile portions of the metal lead become thinner and thinner as current is cycled through the metal lead (**Figure 1B**), and electromigration is even further intensified in this portion. Eventually such leads can break, as shown in **Figure 1C**, resulting in device failures.

The present invention improves reliability of metal leads in structures using low-dielectric constant materials by using dummy vias in contact with metal leads to improve the thermal conductivity of the structure. **Figure 2A** shows a cross-sectional view of a semiconductor wafer **110** having metal leads **114+130** formed on a substrate **112**. The substrate may, for example, contain transistors, diodes, and other semiconductor elements (not shown) as are well known in the art. The substrate **112** may also contain other metal interconnect layers, and typically contains a top insulating oxide layer (to prevent leads from shorting to each other in subsequent metal layers). A first barrier layer is deposited over the substrate **112**. The first barrier layer is preferably comprised of titanium. A first metal interconnect layer is deposited over the first barrier layer. The first metal interconnect layer is preferably comprised of a TiN/AlCu/TiN trilayer, but may also comprise, for example, other aluminum alloy multilayers or monolayers. The first metal interconnect layer and first barrier layer are etched with a predetermined pattern to form etch lines, or metal leads **114+130** (Figure **2A**). Each metal lead **114+130** includes a first metal interconnect portion **114** and a first barrier portion **130**. Some of the metal leads **114+130** may be in close proximity to each other, for example, 1 mm or less apart. The aspect ratio (height/width) of the metal leads is generally at least 1.5, but typically at least 2.0, and more typically at least 3.0.

Low-dielectric constant material **116** is deposited over the metal leads **114+130** and substrate **112** (**Figure 2B**). The low-dielectric constant material **116** is preferably comprised of an OSOG (organic spin-on glass), but may also be comprised of an aerogel, xerogel, or other low-dielectric constant materials which provide a dielectric constant of less than about 3.5, but preferably less than 3.0, and more preferably less than 2.5. The OSOG provides a dielectric constant of about 3.0, and is typically Spun on by a spin-coater and then cured for half an hour to 2 hours at a temperature of 400°C-450°C. The low-dielectric constant material **116** is then removed (e.g., with a timed etch) from at least the tops of metal leads **114+130** (**Figure 2C**). An insulating layer **118** (preferably TEOS silicon dioxide) is applied over the exposed tops of metal leads **114+130** and low-dielectric constant material **116**. Next, the insulating layer **118** may be planarized,

if needed. The insulating layer **118** is patterned (for example, a resist, not shown, may be deposited, exposed, and removed) and etched to leave channels **119** where dummy vias **122+134** will later be formed (**Figure 2D**). Channels for functional vias (not shown) are preferably formed at the same time the channels **119** for dummy vias **122+134** are formed. The channels **119** expose at least the tops of metal leads **114+130** through insulating layer **118**.

Second barrier layer **134** may be deposited over the tops of metal leads **114+130** and insulating layer **118** (**Figure 3A**). Second barrier layer **134** is preferably titanium but may also be a bilayer of Ti/TiN or other metal alloys. Metal layer **120** is deposited over second barrier layer **134**. The metal layer **120** is preferably tungsten and may be deposited with a CVD process, but other metal alloys may be used. The metal layer **120** may then be removed from the second barrier layer **134**, leaving in the channels **119** portions **122** thereof. Thus, dummy vias **122+134** reside in the channels **119** in contact with metal leads **114+130** (**Figure 3B**). Each dummy via **122+134** includes a metal layer portion **122** and a second barrier portion **134**. Since dummy vias **122+134** are comprised of metal, they are excellent thermal conductors. The metal-to-metal contact between the dummy vias **122+134** and the metal leads **114+130** provides an excellent path for thermoconduction. The dummy vias **122+134** conduct away enough of the Joule's heat from, and prevent damage to, the metal leads **114+130** when the device is in operation. Subsequent processing steps may then be performed, e.g., further deposition and etching of semiconductor, insulative and metallic layers. A possible subsequent processing step is shown in **Figure 3C**, where functional metal leads **124+134** are formed in a second metal interconnect layer. The functional metal leads **124+134** are comprised of a second barrier portion **134** and a second metal interconnect portion **124**.

A perspective view of the first embodiment is shown in **Figure 4**. Preferably, a metal lead **114+130** will have several dummy vias **122+134** formed along its length. The more dummy vias **122+134** there are along the metal lead, the more Joule's heat is conducted away from the metal lead **114+130**. For example, in a submicron circuit, dummy vias **122+134** formed every 4 mm along the length of a metal lead **114+130** effectively conducts heat away from the metal lead **114+130**.

A second embodiment of the present invention is shown in a cross-sectional elevational view in **Figure 5**. In this embodiment, dummy vias **122+134** are formed in contact with both the tops and bottoms of metal leads **114**. An advantage of the second embodiment is the ability to conduct away more Joule's heat due to the increase of thermoconductive metal (provided by the dummy vias **122+134**) in contact with metal leads **114**. A perspective view of the second embodiment is shown in **Figure 6**. Dummy vias **122+134** may also be formed only on the bottom of the metal leads **114**, although preferably not on the first metal layer, to avoid damage to transistors and other devices on the underlying circuit.

A third embodiment is shown in **Figure 7**. After the step shown in **Figure 3B**, a second metal interconnect layer is deposited. Dummy leads **126+134** are formed in the second metal interconnect layer, in contact with the dummy vias **122+134**. The dummy leads **126+134** are comprised of a second barrier portion **134** and a second metal interconnect portion **126**. This structure provides more metal (from the dummy vias **122+134** and the dummy leads **126+134**) to conduct away more heat from the metal lead **114+130**. Joule's heat migrates from metal leads **114+130** to dummy vias **122+134** and through dummy vias **122+134** to dummy leads **126+134**. Joule's heat is conducted away from the metal leads **114+130** by both the dummy vias **122+134** and dummy leads **126+134**. (See also U.S. patent application 08/250,983, filed on 5/31/94 by Numata and assigned to Texas Instruments, where dummy leads are formed proximate metal leads). Functional metal leads **124+134** may be formed at the same time dummy leads **126+134** are formed. The functional metal leads **124+134** are comprised of a second barrier portion **134** and a second metal interconnect portion **124**.

A fourth embodiment is shown in **Figure 8**. Multiple layers of dummy vias **122+134** and dummy leads **126** are formed in contact with both the tops and bottoms of metal lead **114+130**, creating a vertical dummy metal path for Joule's heat conduction. (For clarity, first barrier portions **130** of metal leads and second barrier portions **134** of dummy vias are not shown in Figure **8**. Preferably, the sides and bottom of dummy vias contain second barrier portion **134**). This vertical dummy metal path may extend throughout the entire semiconductor wafer, and may terminate at the surface of the wafer to a contact pad which may be connected to other means of heat conduction. This embodiment is especially useful as it can-be relatively easily added after thermal problems are uncovered during, e.g., preproduction testing.

A fifth embodiment of the present invention is shown in **Figure 9**. After the step shown in Figure **2C** of the first embodiment, thermoconductive insulating layer **128**, comprised of AlN, for example, is deposited over the tops of metal leads **114+130** and low dielectric constant material **116**. The thermoconductive insulating layer **128** is patterned and etched to leave channels. A second barrier layer is deposited over the tops of metal leads **114+130** and thermoconductive insulating layer **128**. A metal layer is deposited over second barrier layer (as was shown in Figure **3A**). The second barrier layer and metal layer fill the channels to form dummy vias **122+134** in thermoconductive insulating layer **128**, in contact with metal leads **114+130**, shown in Figure **9**. (Refer to U.S. patent application 08/251,822 fled on 5/31/94 by Numata for Improving Reliability of Metal Leads in High Speed LSI Semiconductors Using Thermoconductive Dielectric Layer). Joule's heat from metal leads **114+130** is transferred to dummy vias **122+134** and then to thermoconductive insulating layer **128**, improving the thermoconductivity of the structure, and thus improving the reliability of the metal leads. Subsequent processing steps as described in other embodiments may then be performed.

A sixth embodiment is shown in **Figures 10A-10D and 11A-11C**. In this embodiment, first barrier layer **130a**, e.g., comprised of titanium, is deposited over the substrate **112** (**Figure 10A**). A first metal interconnect layer **114a** is deposited

over the first barrier layer **130a**. Preferably, the first metal interconnect layer **114a** is comprised of a trilayer of TiN/AlCu/TiN. The trilayer is formed by first depositing titanium nitride over the first barrier layer using a CVD (chemical vapor deposition) process. Second, AlCu is deposited on the titanium nitride using a sputter process; and third, titanium nitride is deposited over the AlCu with a CVD process.

Next, metal leads **114+130** are formed by selective removal of portions of the first metal interconnect layer **114a** and the first barrier layer **130a** (as shown in phantom), leaving portions of the substrate **112** exposed (Figure **10A**). Each metal lead **114+130** includes a first metal interconnect portion **114** and a first barrier portion **130**. A thin insulating layer **132**, for example, TEOS silicon dioxide, is deposited over metal leads **114+130** and exposed portions of the substrate **112 (Figure 10B)**. Low-dielectric constant material **116**, preferably comprised of OSOG, is deposited over the thin insulating layer **132 (Figure 10C)** and may be planarized. Insulating layer **118**, preferably TEOS silicon dioxide, is deposited over low-dielectric constant material **116**. Insulating layer **118**, low-dielectric constant material **116** and thin insulating layer **132** are patterned and etched to form channels **119** where dummy vias **122+134** will be formed (Figure **10D**). Second barrier layer **134** (preferably a bilayer of Ti/TiN, where the Ti is deposited first) is deposited over insulating layer **118**, the tops of metal leads **114+130** and the exposed portions of low-dielectric constant material **116** (Figure **11A**). Metal layer **120** is deposited over second barrier layer **134** (Figure **11B**). Metal layer **120** fills channels **119** to form dummy vias **122+134**. A top portion of metal layer **120** is removed, exposing portions of second barrier layer **134** residing on top of insulating layer **118**, and forming dummy vias **122+134** (Figure **11C**). Each dummy via **122+134** includes a metal layer portion **122** and a second barrier portion **134**. Portions of second barrier layer **134** residing on top of insulating layer **118** are left intact until the next metal interconnect layer is deposited, so that the second barrier layer **134** acts as a thin metal barrier for both the dummy vias **122+134** as well as subsequently-formed functional metal leads **124+134** (for example, as shown in Figure **7**).

An advantage of dummy vias **122+134** is their ability to create a vertical path of heat conduction in a semiconductor circuit. This is beneficial to scaled-down circuits where real estate in the horizontal direction is scarce.

An advantage of the present invention over using only dummy leads (as in U.S. patent application 08/250,983 by Numata) is that In some circuits, there may not be room to form dummy leads proximate to metal leads. Also, the dummy leads, although proximate the metal leads, have a dielectric material residing between the dummy leads and the metal leads: thus, dummy vias, which have a metal-to-metal contact to the metal leads, are superior in conducting away the Joule's heat from the metal leads.

An advantage of the present invention over using only a thermoconductive insulating layer to conduct away some of the Joule's heat (as in U.S. patent application 08/251,822 by Numata) is that no additional steps are required to produce the dummy vias **122+134**. Typically, functional vias are made between metal layers of an integrated circuit, and the dummy vias can be formed when the functional vias are formed.

The present invention can also be used on semiconductors using other low-dielectric constant materials, such as air gaps, aerogels, xerogels, or fluorinated silicon oxide, for example. To reduce capacitive coupling between adjacent leads, low-dielectric constant materials are being investigated, such as pure polymers (e.g., parylene, teflon, polyimide) or organic spin-on glass (OSOG, e.g., silsequioxane or siloxane glass). Refer to U.S. Patent No. 4,987,101 issued to Kaanta et al on Jan. 22, 1991 which describes a method for fabricating gas (air) dielectrics; and U.S. Patent No. 5,103,288 issued to Sakamoto on Apr. 7. 1992 which describes a multilayered wiring structure which decreases capacitance by using a porous dielectric.

The novel structure and method involving the use of dummy vias **122+134** to conduct away Joule's heat from metal leads is particularly beneficial to very compact circuits having no room for dummy leads in the same metal interconnect, or in adjacent metal interconnect layers. The present invention is also beneficial to semiconductors having submicron spacing and using low-dielectric constant materials. The dummy vias **122+134** conduct away a portion of the Joule's heat generated in the metal leads, enhancing reliability of metal leads. The invention is particularly beneficial to semiconductors having a combination of metal leads with high aspect ratios (e.g., 2 or greater) and low-dielectric constant materials (especially having a low-dielectric constant of less than 2) which are more thermally insulating.

While the invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description. It is therefore intended that the appended claims encompass any such modifications or embodiments. For example, although the effects of materials having dielectric constants of about 2.5 and concomitant low thermal conductivity's are ameliorated by the present invention, the dummy vias **122+134** hereof are obviously useful to counteract the effects of any inter-lead dielectric material, the use of which may result in heat damage to the leads due to its low thermoconductivity.

Claims

1. A method for forming conductors on a semiconductor device, comprising:
   forming a conductor on a substrate;
   depositing a low-dielectric constant material over the conductor; and

forming a dummy via in contact with said conductor, wherein heat from said conductor is transferable to said dummy via and conducted away from said conductor.

2. The method of Claim 1, further comprising depositing a low-dielectric constant material having a dielectric constant of less than about 3.5.

3. The method of Claims 1 - 2 , further comprising forming the dummy via prior to said conductor.

4. The method of Claims 1 - 3, further comprising forming a conductor having an aspect ratio greater than 1.5.

5. The method of Claims 1 - 4, further comprising depositing an insulating layer over at least said low-dielectric constant material, wherein said dummy via is formed in said insulating layer.

6. The method of Claim 5, further comprising depositing the insulating layer such that said layer has a conductivity greater than the conductivity of said low-dielectric constant material.

7. The method of Claims 1 - 6, further comprising forming a dummy conductor contact with said dummy via..

8. The method of Claims 1 - 7, further comprising:
depositing an interconnect layer on a substrate;
etching said interconnect layer in a predetermined pattern to form the conductor.

9. The method of Claims 1 - 8, further comprising:
etching said insulating layer to leave a channel in said insulating layer abutting a surface of said conductor; and
depositing a conductive layer over said insulating layer to fill said channel to form a dummy via in contact with said surface of said conductors.

10. The method of Claims 1 - 9, further comprising forming a plurality of conductors.

11. The method of Claims 1-10, further comprising forming a plurality of dummy vias.

12. A semiconductor device, comprising:
at conductor formed on a substrate;
a low-dielectric constant material deposited over said conductor; and
a dummy via in contact with said conductor, wherein heat from said conductor is transferable to said dummy via, and said dummy via is capable of conducting away said heat from said conductor.

13. The semiconductor device of Claim 12, further comprising a dummy conductor in contact with said dummy via, wherein said dummy conductor is capable of conducting away said heat from said conductor.

14. The semiconductor device of Claims 12 - 13, further comprising an insulating layer in contact with at least said low-dielectric constant material, wherein said dummy via is formed within said insulating layer.

15. The semiconductor device of Claims 12 - 14, wherein said insulating layer is comprised of a thermoconductive material comprising AlN, Si_3N_4, or both.

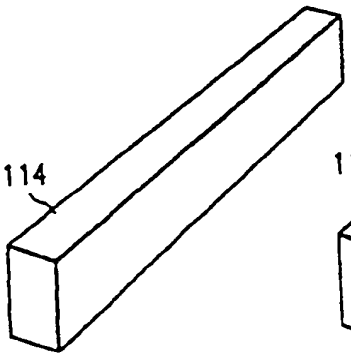

FIG. 1A

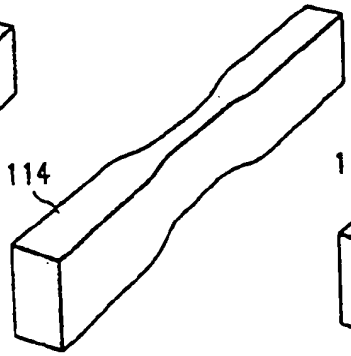

FIG. 1B

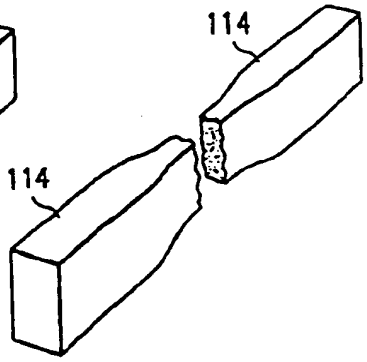

FIG. 1C

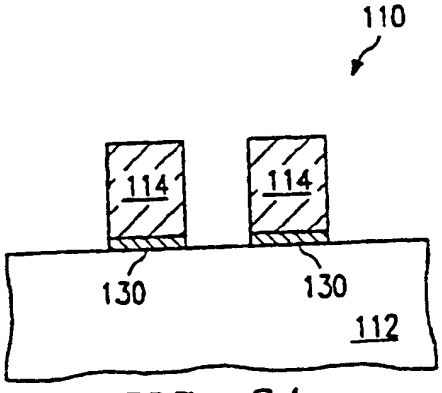

FIG. 2A

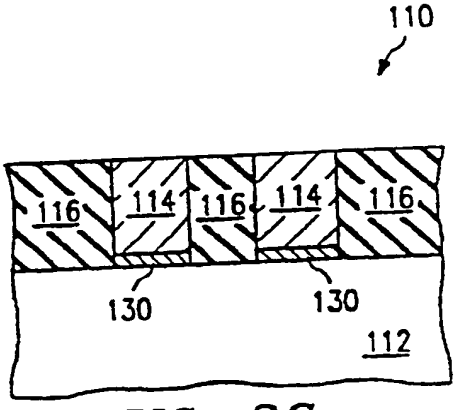

FIG. 2C

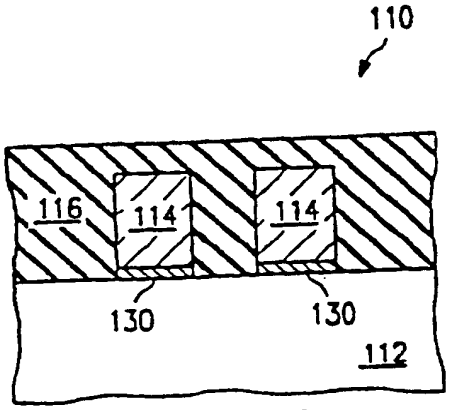

FIG. 2B

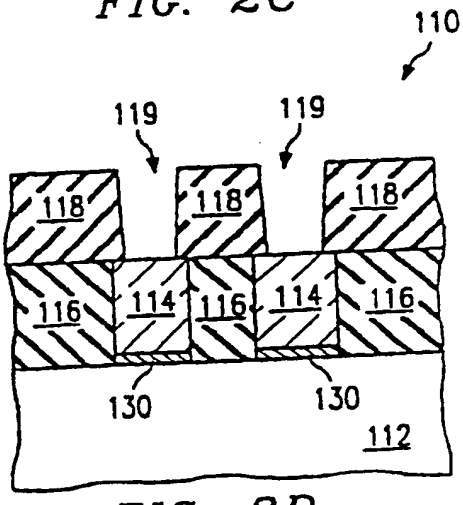

FIG. 2D

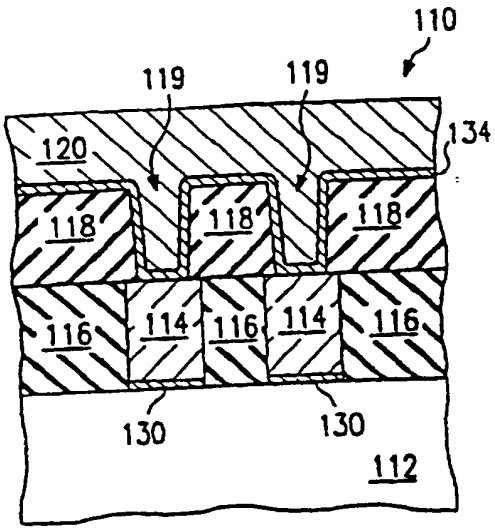

FIG. 3A

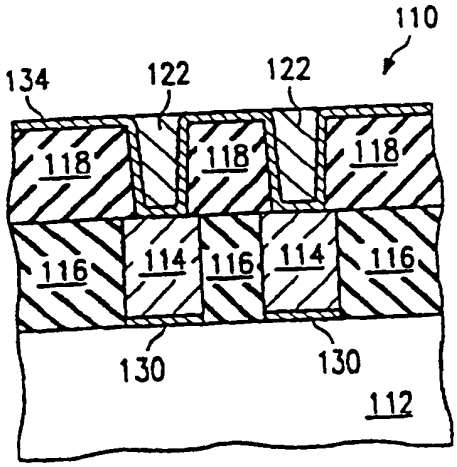

FIG. 3B

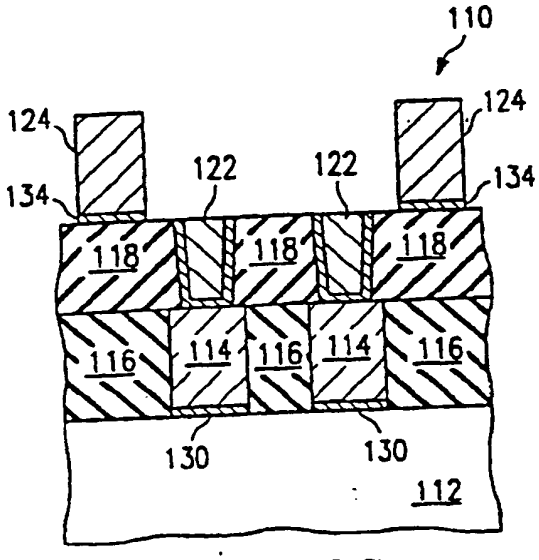

FIG. 3C

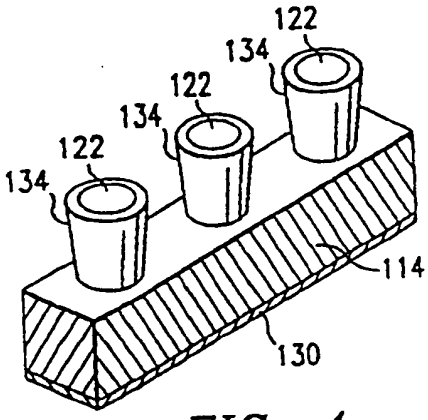

FIG. 4

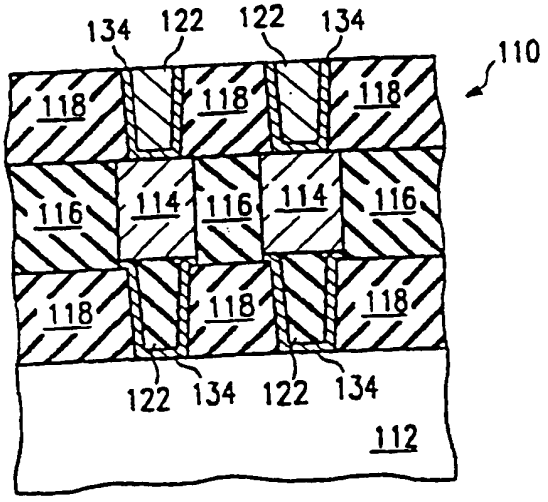

FIG. 5

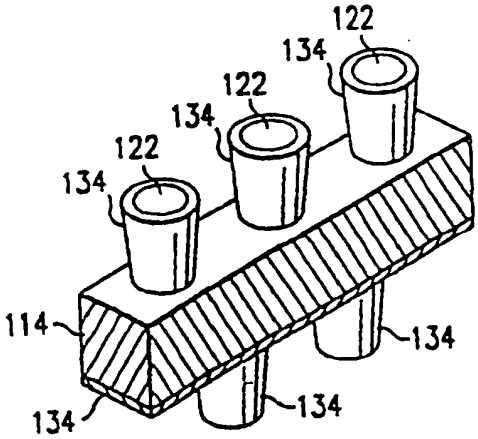

FIG. 6

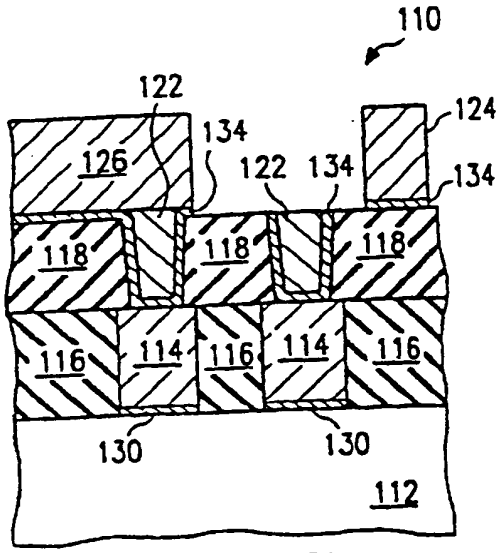

FIG. 7

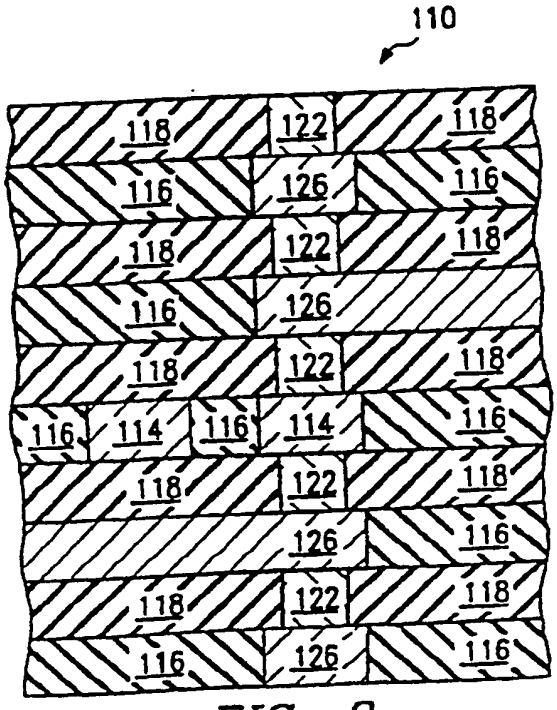

FIG. 8

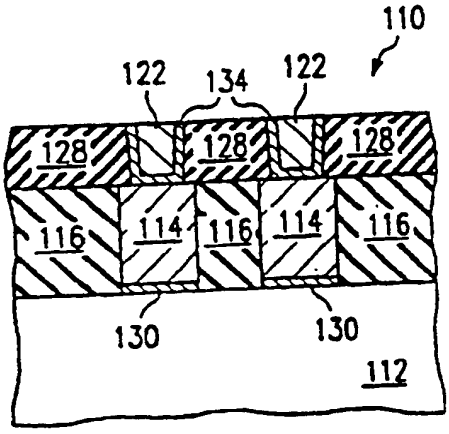

FIG. 9

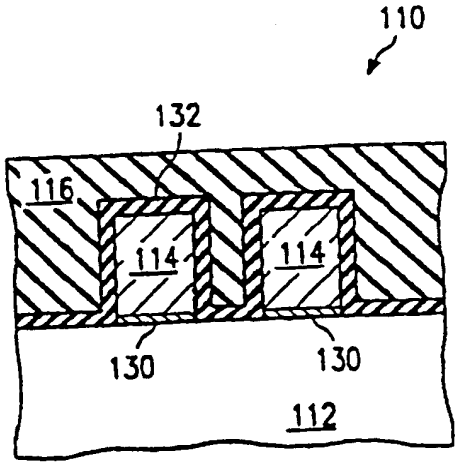

FIG. 10C

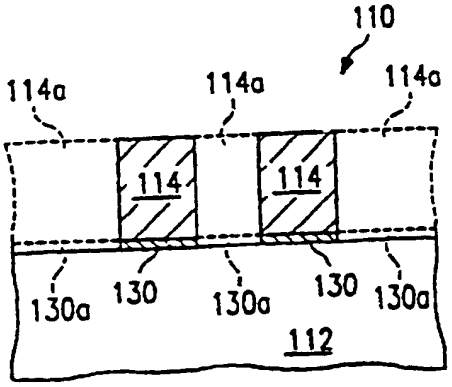

FIG. 10A

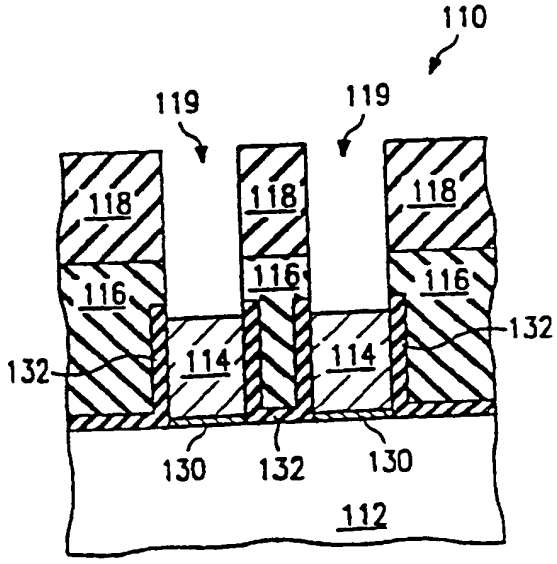

FIG. 10D

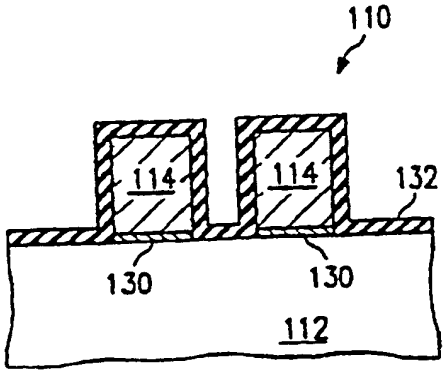

FIG. 10B

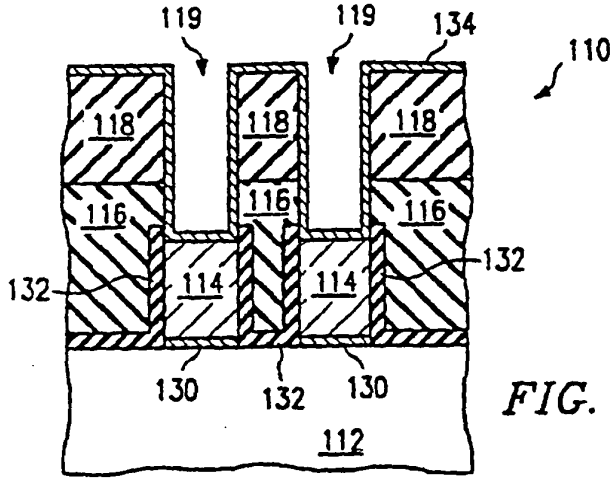

FIG. 11A

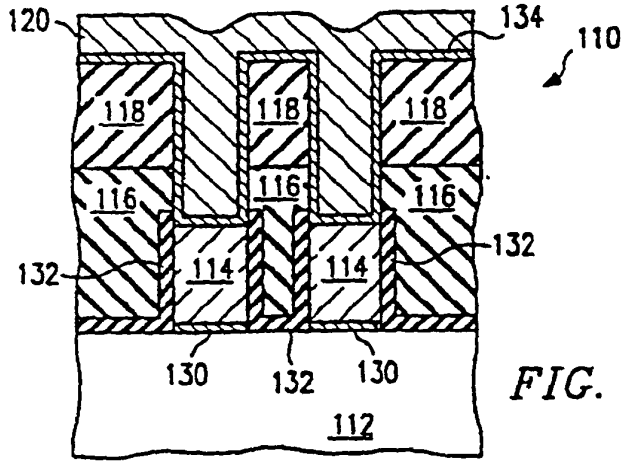

FIG. 11B

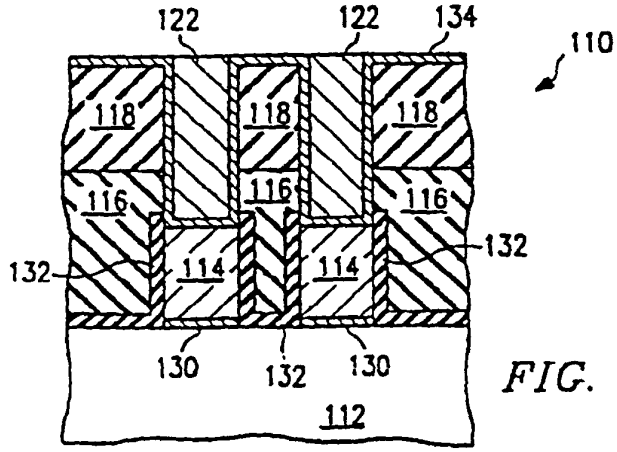

FIG. 11C

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 692 824 A3

(12) EUROPEAN PATENT APPLICATION

(88) Date of publication A3:
16.07.1997 Bulletin 1997/29

(43) Date of publication A2:
17.01.1996 Bulletin 1996/03

(21) Application number: **95111148.3**

(22) Date of filing: **14.07.1995**

(51) Int. Cl.[6]: **H01L 23/522**

(84) Designated Contracting States:
DE FR GB IT NL

(30) Priority: **15.07.1994 US 275570**

(71) Applicant: **TEXAS INSTRUMENTS INCORPORATED**
Dallas, Texas 75243 (US)

(72) Inventors:
- **Numata, Ken**
  Dallas, TX 75240 (US)
- **Houston, Kay L.**
  Richardson, TX 75080 (US)

(74) Representative: **Brown, Angela Mary et al**
Texas Instruments Limited,
Kempton Point,
68 Staines Road West
Sunbury on Thames, Middlesex TW16 7AX (GB)

(54) Improvements in and relating to semiconductor devices

(57) A semiconductor device (and method of manufacturing thereof) having metal leads **(114+130)** with improved reliability, comprising metal leads **(114+130)** on a substrate **112**, a low-dielectric constant material **(116)** at least between the metal leads **(114+130)**, and dummy vias **(122+134)** in contact with the metal leads **(114+130)**. Heat from the metal leads **(114+130)** is transferable to the dummy vias **(122+134)**, and the dummy vias **(122+134)** are capable of conducting away the heat. The low-dielectric constant material **(116)** may have a dielectric constant of less than about 3.5. An advantage of the invention is to improve reliability of metal leads in circuits using low-dielectric constant materials, especially in scaled-down circuits that are compact in the horizontal direction.

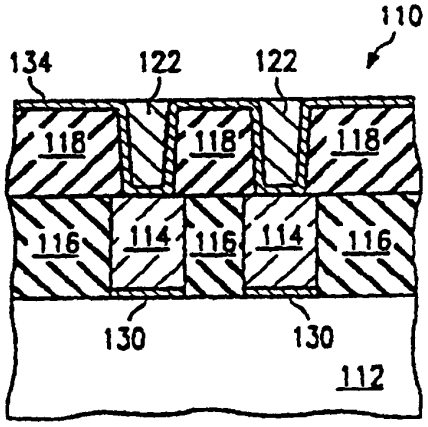

FIG. 3B

EP 0 692 824 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 95 11 1148

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X A	US 5 229 643 A (OHTA HIROYUKI ET AL) 20 July 1993 * column 8, line 1 - line 35 * * column 11, line 21 - column 12, line 21 * * column 21, line 65 - column 23, line 28; figures 1,2,5-7,32,34 *	1,2,7-13 5,14	H01L23/522
A	EP 0 465 197 A (GEN ELECTRIC) 8 January 1992 * page 6, line 52 - page 7, line 13 *	1,2	
D,A	US 5 103 288 A (SAKAMOTO MITSURU ET AL) 7 April 1992 * the whole document *	1,2	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6) H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	7 May 1997	Zeisler, P

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference	**FOR FURTHER ACTION** see Notification of Transmittal of International Search Report (Form PCT/ISA/220) as well as, where applicable, item 5 below.	
M4065.0247/P		
International application No.	International filing date *(day/month/year)*	(Earliest) Priority Date *(day/month/year)*
PCT/US 01/ 11636	10/04/2001	11/04/2000
Applicant		
MICRON TECHNOLOGY, INC.		

This International Search Report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This International Search Report consists of a total of 3 sheets.

[X] It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

   a. With regard to the **language,** the international search was carried out on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.

   [ ] the international search was carried out on the basis of a translation of the international application furnished to this Authority (Rule 23.1(b)).

   b. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international search was carried out on the basis of the sequence listing :

   [ ] contained in the international application in written form.

   [ ] filed together with the international application in computer readable form.

   [ ] furnished subsequently to this Authority in written form.

   [ ] furnished subsequently to this Authority in computer readble form.

   [ ] the statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

   [ ] the statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished

2. [ ] **Certain claims were found unsearchable** (See Box I).

3. [ ] **Unity of invention is lacking** (see Box II).

4. With regard to the **title,**

   [X] the text is approved as submitted by the applicant.

   [ ] the text has been established by this Authority to read as follows:

5. With regard to the **abstract,**

   [X] the text is approved as submitted by the applicant.

   [ ] the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box III. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. The figure of the **drawings** to be published with the abstract is Figure No. 8

   [X] as suggested by the applicant.

   [ ] None of the figures.

   [ ] because the applicant failed to suggest a figure.

   [ ] because this figure better characterizes the invention.

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 01/11636

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L23/367 H01L23/373 H01L23/532

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 016 000 A (MOSLEHI MEHRDAD M) 18 January 2000 (2000-01-18) column 12, line 32 -column 16, line 53; figure 15 --- -/--	1,2,7,8, 14,15, 18,19, 21,47, 48, 50-55,57

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
25 March 2002	03/04/2002

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Ploner, G

1

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 01/11636

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 874 777 A (OHMI TADAHIRO ET AL) 23 February 1999 (1999-02-23) column 8, line 55 -column 9, line 6 column 10, line 31-43 column 17, line 41-63; figures 4,10,12,14-17	15,16, 18,19, 21,29, 33,35, 36,38, 39,41, 44,47, 48, 50-55,57
X	EP 0 260 906 A (FUJITSU LTD) 23 March 1988 (1988-03-23) the whole document	18,19, 21,22, 26, 28-30, 33,35, 47,48, 50, 52-54,57
X	US 5 670 387 A (SUN SHIH-WEI) 23 September 1997 (1997-09-23) column 2, line 33-47 column 5, line 51 -column 6, line 15; figure 13	18,19, 21,36, 38,44, 47,48, 50, 52-54,57
X	EP 0 692 824 A (TEXAS INSTRUMENTS INC) 17 January 1996 (1996-01-17) page 3, line 33 -page 4, line 13 page 5, line 40 -page 6, line 4; figures 8,9	47-57
A		1-46
X	US 5 476 817 A (NUMATA KEN) 19 December 1995 (1995-12-19) the whole document	53,55,57
A		1-52,54, 56

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 01/11636

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6016000 A	18-01-2000	EP 1000440 A1	17-05-2000
		JP 2002506577 T	26-02-2002
		WO 9954934 A1	28-10-1999
		US 6124198 A	26-09-2000
US 5874777 A	23-02-1999	JP 9129725 A	16-05-1997
		WO 9624159 A1	08-08-1996
		TW 383481 B	01-03-2000
EP 0260906 A	23-03-1988	JP 1059938 A	07-03-1989
		JP 63073645 A	04-04-1988
		DE 3784605 D1	15-04-1993
		DE 3784605 T2	17-06-1993
		EP 0260906 A2	23-03-1988
		KR 9007147 B1	29-09-1990
US 5670387 A	23-09-1997	NONE	
EP 0692824 A	17-01-1996	US 5625232 A	29-04-1997
		EP 0692824 A2	17-01-1996
		JP 8083797 A	26-03-1996
		US 5675187 A	07-10-1997
US 5476817 A	19-12-1995	JP 8070005 A	12-03-1996
		US 5519250 A	21-05-1996